Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-11 (Canceled)

Claim 12 (Currently Amended): A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate futher having an elongate opening defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of said plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of said substrate;

a plurality of electrodes located on the surface of said semiconductor chip and aligned with said elongate opening of said substrate;

a plurality of wires extending within said elongate opening of said substrate, first ends of said plurality of wires being respectively bonded to said plurality of electrodes and second ends of said plurality of wires being respectively bonded to corresponding ones of said plurality of connecting patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns;

a resist which covers side walls of said plurality of connecting patterns and second ends of said plurality of connecting patterns; and

a plurality of external connecting terminals respectively bonded to the second ends of said plurality of connecting patterns through said resist,

wherein said resin extends out of said elongate opening beyond a height of said plurality of connecting patterns at which said plurality of external connecting terminals are bonded.

Claim 13 (Previously Presented): A semiconductor device as claimed in claim 12, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein said plurality of connecting patterns extend continuously from the upper plate to the lower plate such that the first ends of said plurality of connecting patterns are located on the upper plate.

Claim 14 (Previously Presented): A semiconductor device as claimed in claim 12, wherein said elongate opening is smaller than said semiconductor chip.

Claim 15 (Previously Prestented): A semiconductor device according to claim 12, further comprising a bonding material formed on an entirety of the first surface of said substrate, wherein said semiconductor chip is mounted on the first surface of said substrate via said bonding material.

Claim 16 (Previously Presented): A semiconductor device according to claim 12, wherein said plurality of external connecting terminals are solder balls.

Claim 17 (Canceled)

Claim 18 (Currently Amended): A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate futher having an elongate opening defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of said plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of said substrate;

a plurality of electrodes located on the surface of said semiconductor chip and aligned with said elongate opening of said substrate;

a plurality of wires extending within said elongate opening of said substrate, first

ends of said plurality of wires being respectively bonded to said plurality of electrodes and second ends of said plurality of wires being respectively bonded to corresponding ones of said plurality of connecting patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns;

a resist which covers side walls of said plurality of connecting patterns and second ends of said plurality of connecting patterns; and

a plurality of external connecting terminals respectively bonded to the second ends of said plurality of connecting patterns through said resist ~~according to claim 12~~,

wherein said resin extends out of said elongate opening less than a height of said plurality of connecting patterns at which said plurality of external connecting terminals are bonded.

Claim 19 (Currently Amended): A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having first and second elongate openings defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of said plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of said substrate;

a plurality of electrodes located on the surface of said semiconductor chip, each of said plurality of electrodes aligned with one of said first and second elongate openings of said substrate;

a plurality of wires each extending within one of said first and second elongate openings of said substrate, first ends of said plurality of wires being respectively bonded to said plurality of electrodes and second ends of said plurality of wires being respectively bonded to corresponding ones of said plurality of connecting patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns;

a resist which covers side walls of said plurality of connecting patterns and second ends of said plurality of connecting patterns; and

a plurality of external connecting terminals respectively bonded to the second ends of said plurality of connecting patterns through said resist,

wherein said resin extends out of said first and second elongate openings beyond a height of said plurality of connecting patterns at which said plurality of external connecting terminals are bonded.

Claim 20 (Previously Presented): A semiconductor device as claimed in claim 19, wherein said substrate includes an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and the lower plate, and wherein said plurality of

connecting patterns extend continuously from the upper plate to the lower plate such that the first ends of said plurality of connecting patterns are located on the upper plate.

Claim 21 (Previously Presented): A semiconductor device as claimed in claim 19, wherein said first and second elongate openings are smaller than said semiconductor chip.

Claim 22 (Previously Presented): A semiconductor device according to claim 19, further comprising a bonding material formed on an entirety of the first surface of said substrate, wherein said semiconductor chip is mounted on the first surface of said substrate via said bonding material.

Claim 23 (Previously Presented): A semiconductor device according to claim 19, wherein said plurality of external connecting terminals are solder balls.

Claim 24 (Canceled)

Claim 25 (Currently Amended): A semiconductor device comprising:

a substrate having a first surface and a second surface opposed to the first surface, said substrate further having first and second elongate openings defined therethrough from the first surface to the second surface;

a plurality of connecting patterns located on the second surface of said substrate, each of said plurality of connecting patterns having a first end;

a semiconductor chip having a surface which is mounted to the first surface of said substrate;

a plurality of electrodes located on the surface of said semiconductor chip, each of said plurality of electrodes aligned with one of said first and second elongate openings of said substrate;

a plurality of wires each extending within one of said first and second elongate openings of said substrate, first ends of said plurality of wires being respectively bonded to said plurality of electrodes and second ends of said plurality of wires being respectively bonded to corresponding ones of said plurality of connecting patterns;

a resin which covers said plurality of electrodes, said plurality of wires, and the first ends of said plurality of connecting patterns;

a resist which covers side walls of said plurality of connecting patterns and second ends of said plurality of connecting patterns; and

a plurality of external connecting terminals respectively bonded to the second ends of said plurality of connecting patterns through said resist ~~according to claim 19~~,

wherein said resin extends out of said first and second elongate openings less than a height of said plurality of connecting patterns at which said plurality of external connecting terminals are bonded.